Consumer Microcircuits Limited

PRODUCT INFORMATION

FX106 Audio Processor for NBFM Radio

With compliments of Island Labs

Publication D/106/1 May 1985
PROVISIONAL ISSUE

Features

- Dual Audio BP Filters
- Dual LP Data Filters
- Peak Limiter and Post Filter
- Pre-emphasis and De-emphasis
- 5-Volt Low Power CMOS

Applications

- Cordless Telephones
- Full Duplex Mobile Radio
- Portable Two-way Radio
- Telephony
- Intercoms

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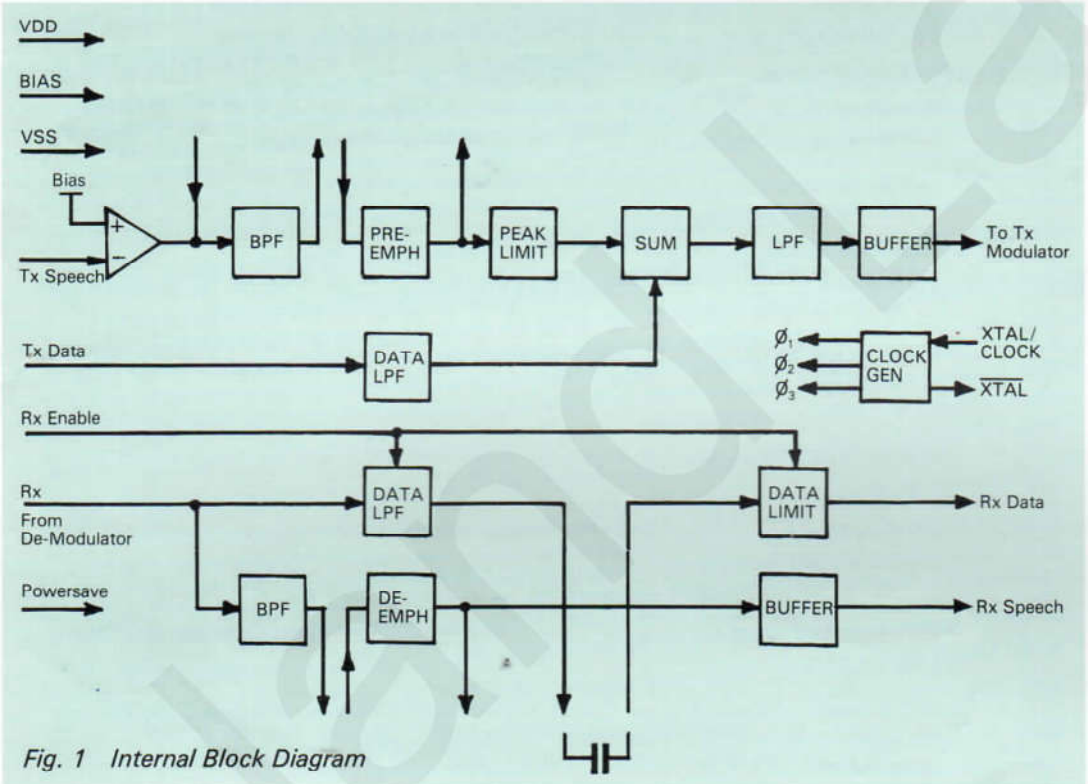

Fig. 1 Internal Block Diagram

FX106

Brief Description

The FX106 is an audio frequency processing circuit designed for use in narrow band FM transceivers. The single chip contains circuit elements to process voice frequencies and sub-audio data in full duplex operation. The low-power CMOS process operating from a single supply and choice of DIL or surface mounted packages makes the device suitable for portable or fixed applications. The transmit section contains an input amplifier with facilities for external gain adjustment, bandpass filter, pre-emphasis amplifier, peak deviation limiter, post-limiter filter, output buffer and transmit data filter. The receiver section contains a bandpass filter, de-emphasis amplifier, output buffer, receiver data filter and limiter. Facilities are provided to disable the operation of the circuit except the receiver data channel, thereby saving power consumption in the standby mode.

The FX106 makes extensive use of switched capacitor filter techniques and all sampling clocks are derived from a clock oscillator divider circuit using an externally connected 1MHz crystal or ceramic resonator.

Pin Number		Function
FX106J	FX106LV1	
		See Figures 2 and 3
1	1	**$\overline{\text{Xtal}}$:** Inverting output of the on-chip crystal oscillator.
2	2	**Powersave:** Internally pulled to Vdd, a logic '0' applied to this pin will disable all parts of the circuit except the data LPF and data limiter.
3	3	**Rx enable:** Internally pulled to Vdd, a logic '0' applied to this pin will disable the data LPF and data limiter.
4	4	**Pre-emph. O/P:** } These pins are used to connect the external components required for the pre-emphasis frequency response.
5	5	**Pre-emph. I/P:** }
6	6	**Tx Bandpass O/P:** }
7	8	**Gain adjust:** } These pins are used to set the gain of the Tx input amplifier by externally connected resistors.
8	9	**Tx speech I/P:** }
9	11	**Analogue data O/P:** This pin outputs the received data signal after filtering, normally connected to Pin 14 (16) via an external capacitor.
10	12	**Vss:** Negative supply.
11	13	**Tx data I/P:** This pin is the input to the Tx data filter.
12	14	**Rx data O/P:** This pin is the logic level output of the limiter used to limit the received analogue data signal.
13	15	**V bias:** Vdd/2 bias pin, externally decoupled by capacitor.
14	16	**Data limiter I/P:** Input of the data limiter, normally coupled via capacitor to Rx data LPF output.
15	17	**Rx speech + data I/P:** This is the input to the Rx bandpass filter and Rx data LPF.
16	18	**Rx speech O/P:** This is the output of the buffer amplifier following the de-emphasis amplifier.
17	19	**Rx bandpass O/P:** } These pins are used to connect the external components required for the de-emphasis frequency response.
18	20	**De-emphasis I/P:** }
19	21	**De-emphasis O/P:** }
20	22	**Tx speech + data O/P:** This is the combined speech and data output following summation and post limiter filtering.
21	23	**Vdd:** Positive supply.
22	24	**Xtal/Clock:** Input to the on-chip crystal oscillator, a 1MHz crystal or ceramic resonator is connected between this pin and pin 1. This input is used as the input from an external 1MHz clock oscillator.

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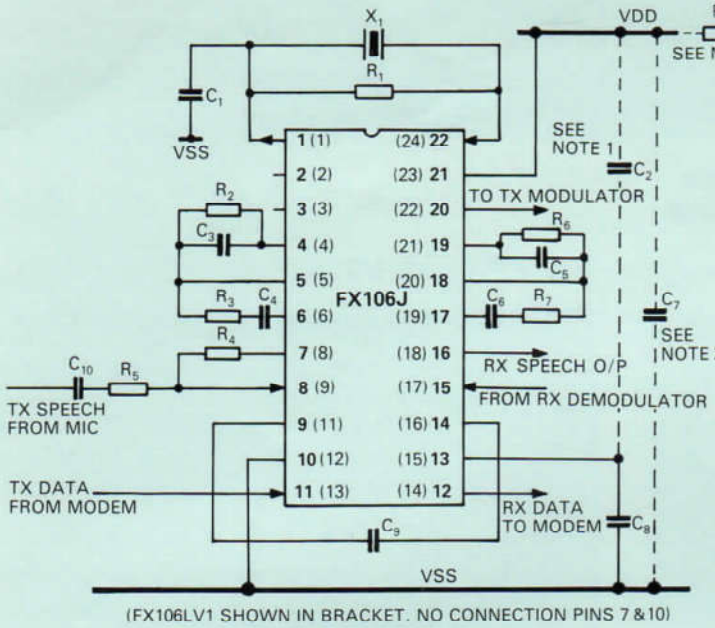


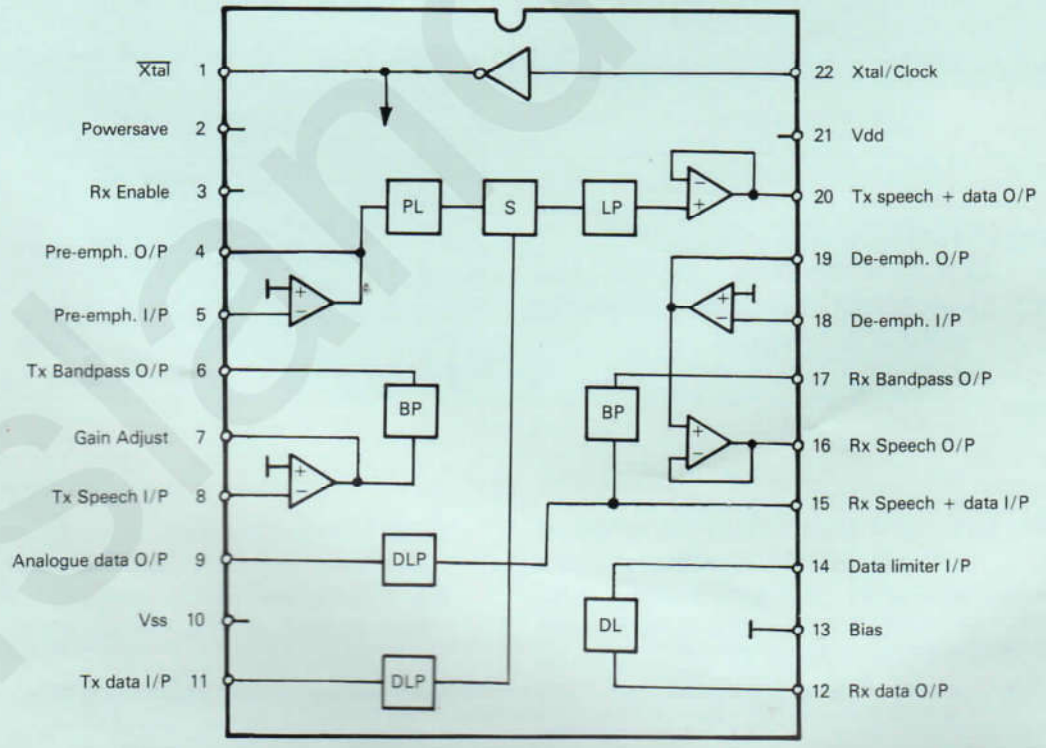
COMPONENT REFERENCES*			
Component	Recommended Unit Value	Component	Recommended Unit Value
R_1	1M	C_1	33p
R_2	82k	C_2	0.1µ
R_3	7.5k	C_3	220p
R_4	1M	C_4	2n
R_5	100k	C_5	10n
R_6	51k	C_6	1.5µ
R_7	13k	C_7	0.1µ
R_8	(See Note 3)	C_8	0.1µ
X_1	1MHz crystal	C_9, C_{10}	0.1µ

*TOLERANCE:
Resistors ±10%
Capacitors ±20%

NOTES:

1. *Bias may be decoupled to VSS and VDD using C_2, C_8 when input signals are referenced to the bias pin. For input signals referenced to VSS, decouple Bias to VSS using C_8 only.*
2. *Use C_7, when input signals are referenced to VSS, to decouple VDD.*
3. *Use R_8 to assist decoupling of high frequency power supply noise (R_8 C_7 typically 300µs)*

Fig. 2 External Component Connections



KEY:
PL — Peak limiter
S — Summing amplifier
BP — Bandpass filter (speech), 300Hz – 3kHz
LP — Lowpass filter (speech + data), 3kHz
DLP — Data lowpass filter, 100Hz

Fig. 3 Functional Block Diagram

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		−0.3V to 7.0V
Input voltage at any pin (ref VSS = OV)		−0.3V to (VDD + 0.3V)
Output sink/source current (total)		20mA
Operating temperature range:	FX106J	−30°C to + 85°C
	FX106LV1	−30°C to + 70°C
Storage temperature range:	FX106J	−55°C to +125°C
	FX106LV1	−40°C to + 85°C

Operating Limits

All characteristics measured using the following parameters unless otherwise specified.
VDD = 5V, T_{amb} = 25°C, ϕ = 1MHz, Δf_{ϕ} = 0, reference input frequency = 1kHz (0dB)

Characteristics	See Note	Min	Typ	Max	Unit
D.C. Characteristics					
Supply voltage		4.5	5.0	5.5	V
Supply current:			5.0		mA
Supply current (standby)			500		μA
Input logic '1'		3.5			V
Input logic '0'				1.5	V
Output logic '1'	1	4.0			V
Output logic '0'	1			1.0	V
A.C. Characteristics					
Input impedance					
Input amplifiers		1			MΩ
Data Input		100			kΩ
Output impedance					
Output buffer amplifier				10	Ω
Pre- and de-emphasis amplifier				800	Ω
Data limiter				800	Ω
Open loop voltage gain					
All amplifiers	2	35			dB
Filter Characteristics					
Bandpass filter gain at 1kHz	3	−1		+1	dB
Bandpass filter frequency response	3				
$f \leqslant$ 100Hz		−25	−30		dB
$f \leqslant$ 300Hz		−3		+1	dB
500Hz $\leqslant f \leqslant$ 3000Hz		−0.75		+0.75	dB
$f \leqslant$ 9000Hz		−15			dB
Lowpass filter gain at 1kHz	3	3		5	dB
Lowpass filter frequency response	3				
$f \leqslant$ 3000Hz		−0.75		+0.75	dB
f = 3400Hz		−2		+1	dB
$f \leqslant$ 9000Hz		−15			dB
Transmit data filter gain	4	−3		−1	dB
Receive data filter gain	4	15	20	25	dB
Data filter frequency response	4				dB
$f \leqslant$ 100Hz		−0.75		+0.75	dB
$f \geqslant$ 300Hz		−30	−35	−40	dB
Maximum a.c. signal for all filters		4.0			V pk-pk
Peak limiter Characteristic					
Maximum a.c. signal before clipping				3.2	V pk-pk
Data Limiter Characteristic					
Sensitivity	5			40	mV r.m.s.

Note: 1. I_{source} = 100μA, I_{sink} = 100μA
2. *F = 1kHz, V_{in} = 7.0mV r.m.s.*
3. *V_{in} = 300mV r.m.s.*
4. *Reference frequency = 85Hz (0dB), V_{in} = 300mV r.m.s.*
5. *Input voltage required to produce logic levels (note 1) at the output, output duty cycle 50 ± 5%. Input sinewave at 85Hz a.c. coupled.*

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Typical Frequency Response Characteristics

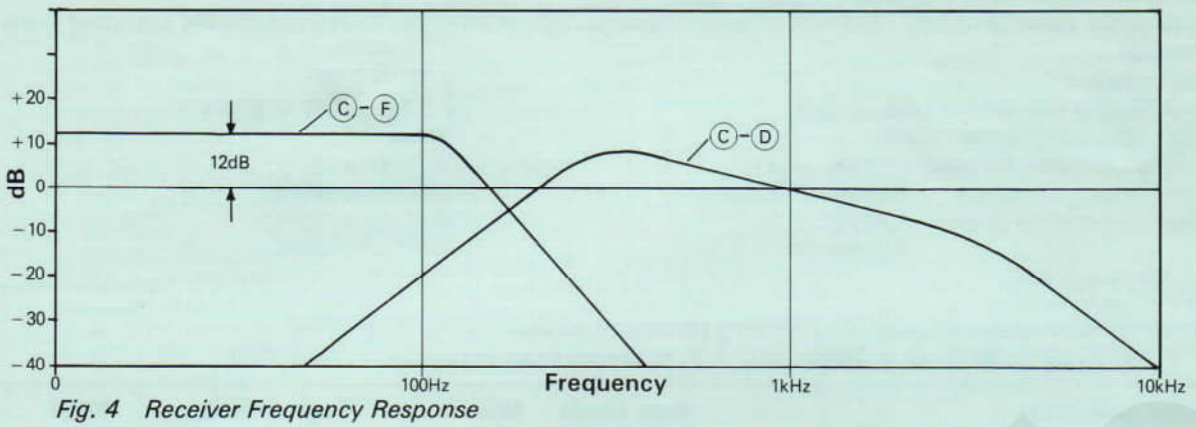


Fig. 4 Receiver Frequency Response

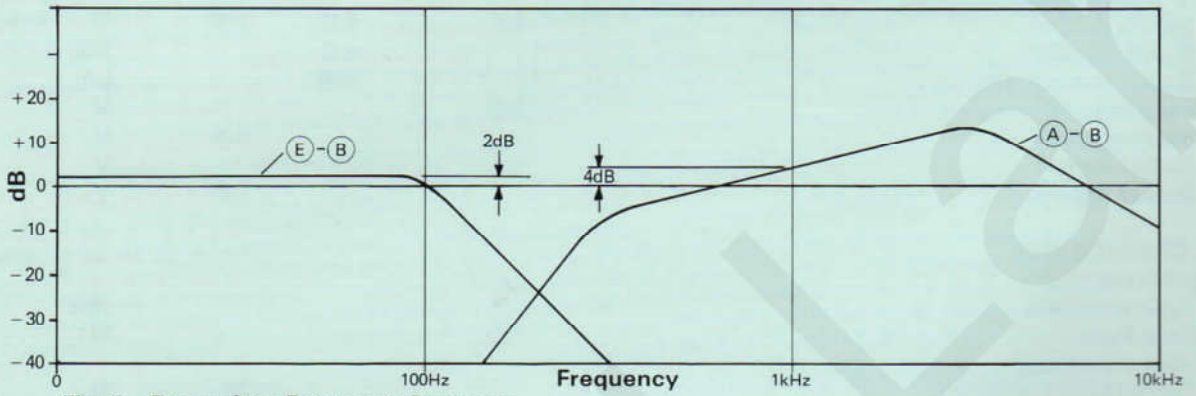


Fig. 5 Transmitter Frequency Response

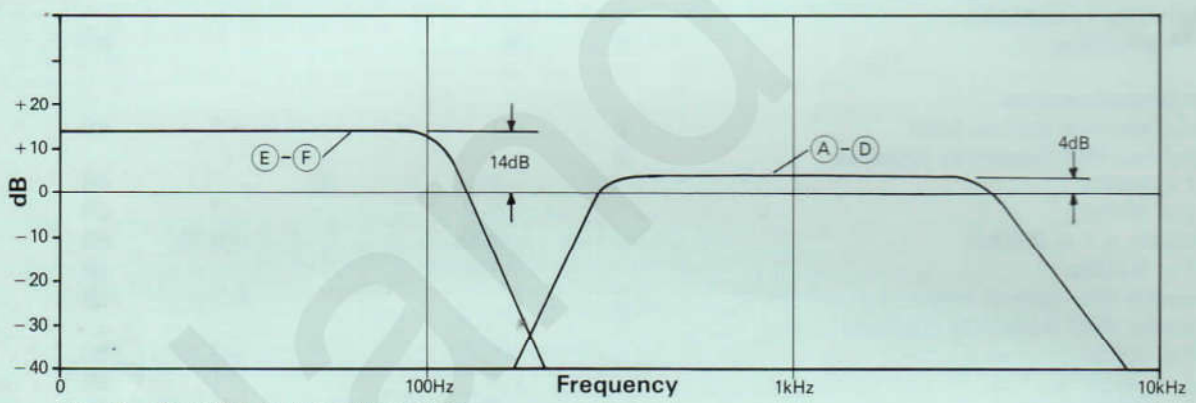


Fig. 6 Overall Frequency Response

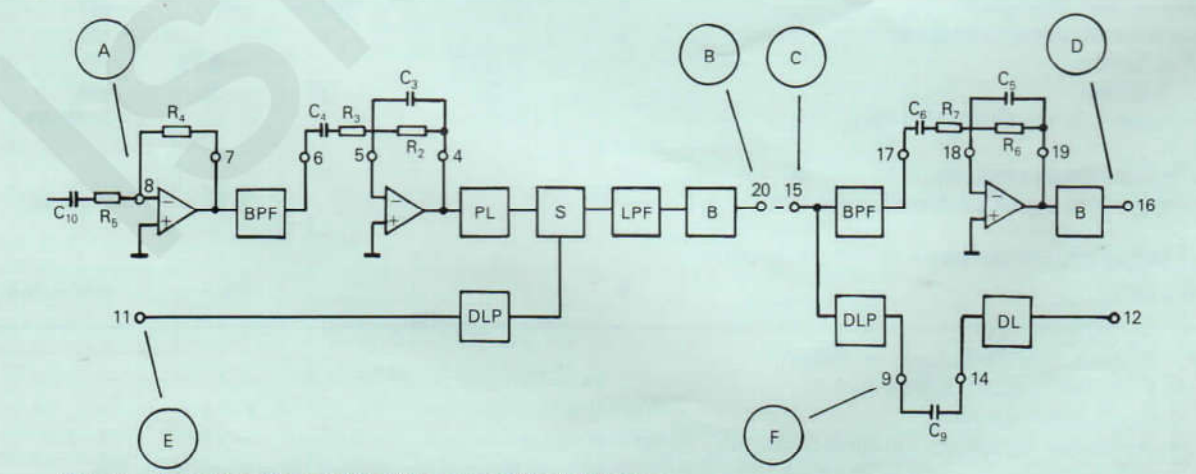
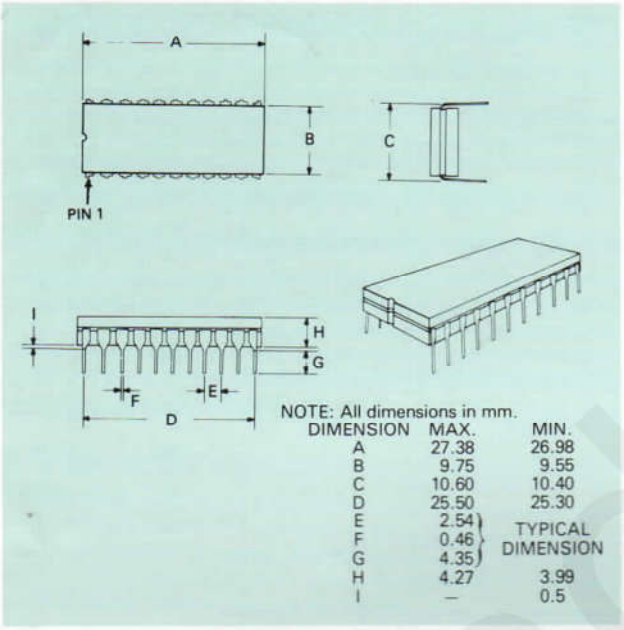


Fig. 7 Complete Transmitter/Receiver Block Diagram.

Package Outlines

The cerdip package of the FX106J is shown in *Figure 8.* The FX106LV1 of *Figure 9* is supplied in a conductive tray.
The FX106LV1 has an indent (spot) adjacent to Pin 1 and a chamfered corner between Pins 3 and 4 to allow complete identification. Pins number counter-clockwise when viewed from the top (indent side).

Fig. 8 ***FX106J*** *D.I.L. Package*



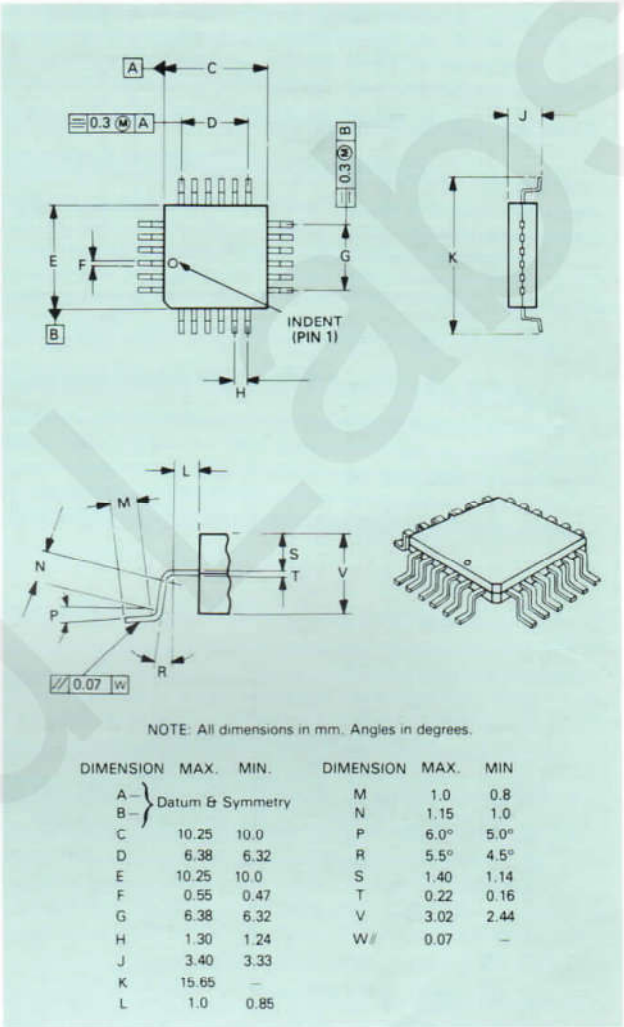
NOTE: All dimensions in mm.

DIMENSION	MAX.	MIN.
A	27.38	26.98
B	9.75	9.55
C	10.60	10.40
D	25.50	25.30
E	2.54	TYPICAL DIMENSION
F	0.46	TYPICAL DIMENSION
G	4.35	TYPICAL DIMENSION
H	4.27	3.99
I	—	0.5

Handling Precautions

The FX106J/LV1 is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent static discharges which can cause damage.

Fig. 9 ***FX106LV1*** *Package*



NOTE: All dimensions in mm. Angles in degrees.

DIMENSION	MAX.	MIN.	DIMENSION	MAX.	MIN
A, B	Datum & Symmetry		M	1.0	0.8
			N	1.15	1.0
C	10.25	10.0	P	6.0°	5.0°
D	6.38	6.32	R	5.5°	4.5°
E	10.25	10.0	S	1.40	1.14
F	0.55	0.47	T	0.22	0.16
G	6.38	6.32	V	3.02	2.44
H	1.30	1.24	W	0.07	—
J	3.40	3.33			
K	15.65	—			
L	1.0	0.85			

Ordering Information

FX106J 22-pin Cerdip D.I.L.
FX106LV1 24-pin quad plastic encapsulated, bent and cropped.

CML does not assume any responsibility for the use of any circuitry described. No circuit patent licences are implied and CML reserves the right at any time without notice to change the said circuitry.

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