Consumer Microcircuits Limited

PRODUCT INFORMATION

FX335/FX335L CTCSS Encoder/Decoder

Publication D/335/2 November 1983
Preliminary
Information

Features

- CTCSS Encoder/Decoder
- Crystal controlled tones
- 38 Field programmable tones
- On-chip filtering to attenuate incoming CTCSS tone
- Low power CMOS
- Includes audio switch
- Choice of package styles
- Meets EIA RS 220A Specifications
  MPT 1306 Specifications

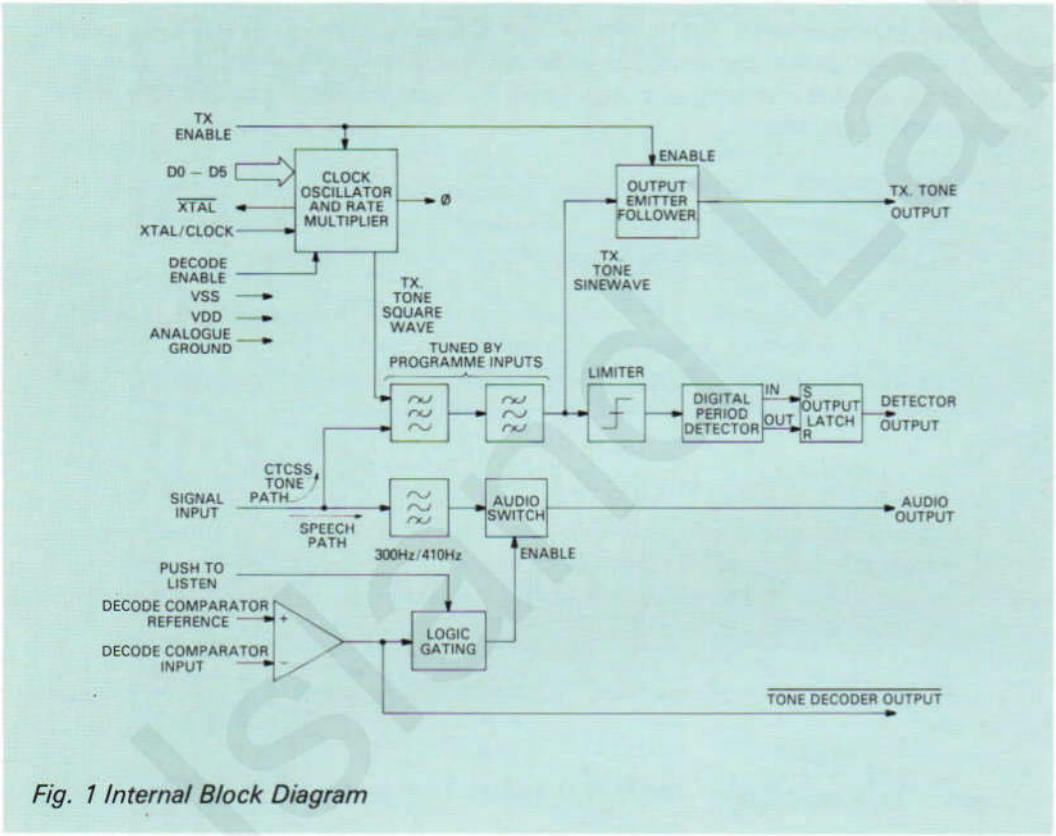


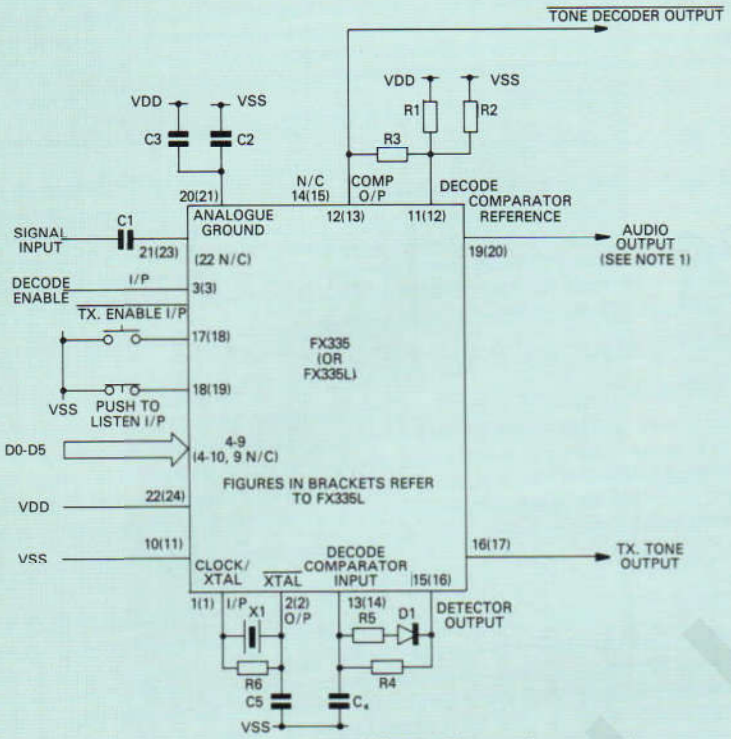
Fig. 1 Internal Block Diagram

FX335
FX335L

Brief Description

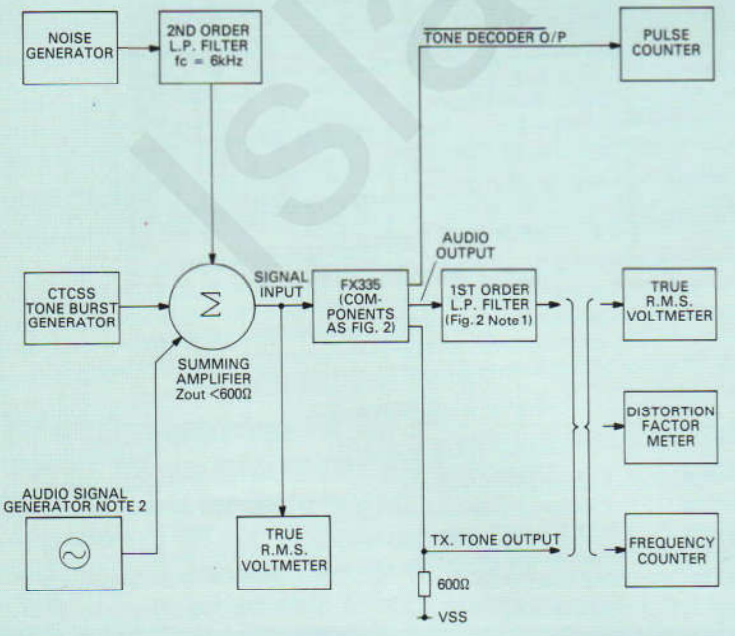
The FX335 is a CMOS CTCSS encoder/decoder used for the generation and detection of 38 sub-audible tones. The sub-audible tone encode/decode functions are all derived from an on-chip crystal oscillator and are digitally programmed by six wire link inputs. The decoder has an on-board switched capacitor high-pass filter used to attenuate the sub-audible tones in the speech path. Also included in the speech path is an audio switch which is activated by the detection of the correct CTCSS tone. Channel monitoring is achieved by the use of a 'push to listen' input. Transmit and receive enable inputs allow the FX335 device to be put in a standby mode, thus reducing supply current.

Pin FX335	Pin FX335L	Description Function
1	1	1MHz XTAL Input: Can also be used to apply an externally derived 1MHz clock input (Clock I/P). The external crystal determines the frequency accuracy of all internal functions.
2	2	$\overline{\text{Xtal}}$ Oscillator Output: (Clock O/P).
3	3	Decode Enable Input: A logic 0 applied to this input will disable the decoder. This can be connected to carrier squelch, if required.
4	4	D5: These six data input lines (D0-D5) are used to programme the encode/decode
5	5	D4: tone frequencies and are internally pulled high to VDD via resistors.
6	6	D3:
7	7	D2:
8	8	D1:
—	9	No connection
9	10	D0:
10	11	VSS: Negative supply.
11	12	Decode Comparator Ref: A split resistor network connected to this input sets the threshold level of the comparator. An additional resistor connected between this input and the comparator output allows for hystersis which reduces jitter under marginal conditions.
12	13	$\overline{\text{Tone Decoder O/P}}$: This is the output of the comparator used to open the analogue gate and can also be used to flag the successful detection of the correct CTCSS tone. **Note:** *This output is active LOW (for decode).*
13	14	Decode Comparator I/P: The tone detector output, when integrated, is applied to this input. A voltage, present at this input, which is higher than the threshold voltage (Pin 11 — FX335) will cause the comparator output to go low and hence open the audio gate, i.e. indicating a succesful decode.
14	15	No connection.
15	16	Detector Output: This logic output is set high by the successful detection of the correct CTCSS tone. To avoid any chatter on this output being superimposed on the audio output, this output is integrated and then applied to the comparator input (Pin 13 — FX335).
16	17	TX Tone O/P: The generated sub-audible tone sinewave is transmitted from this output.
17	18	$\overline{\text{TX Enable I/P}}$: A logic 0 applied to this input will enable the transmitter.
18	19	Push to Listen I/P: This input is internally pulled to VDD. Normally this input would be externally tied to VSS for normal decode operation. Open circuiting this input will manually override the decoder and open the audio gate.
19	20	Audio O/P:
20	21	Analogue ground: Externally decoupled by C_2 and C_3.
—	22	No connection.
21	23	Signal Input: C1 a.c. couples the signals into the device. To avoid injecting unwanted signals into this pin, keep wiring short.
22	24	VDD: Positive Supply.



NOTE *1: A filter may be connected to remove extraneous signals outside audio band. A simple LP filter comprising a 22kΩ resistor and 1nF capacitor can be used if due allowance is made for insertion loss.*

Fig. 2 External Component Connections



NOTE *2: Frequency range 300Hz to 3400Hz.*

Fig. 3 Test Set up

External Components

Component	Value	Tolerance
R1	43kΩ	10%
R2	56kΩ	10%
R3	43kΩ	10%
R4	820kΩ	5%
R5	100kΩ	5%
R6	1MΩ	10%
C1	10nF	20%
C2	0.47μF	20%
C3	0.47μF	20%
C4	0.1μF	10%
C5	33pF	20%
X1	1MHz quartz	
D1	1N914 or similar	

Note: *In high noise level conditions the possible falsing can be reduced by increasing the value of C4; however, this may affect the response time. Discharging C4, when no carrier is present, will inhibit any potential false responses.*

Truth Table 2 Code Programming

Nominal Freq. (Hz)	FX335 Frequency	Δfo%	Programme Inputs D_0	D_1	D_2	D_3	D_4	D_5
67.0	67.05	+.07	1	1	1	1	1	1
71.9	71.90	0.0	1	1	1	1	1	0
74.4	74.35	−.07	0	1	1	1	1	1
77.0	76.96	−.05	1	1	1	1	0	0
79.7	79.77	+.09	1	0	1	1	1	1
82.5	82.59	+.10	0	1	1	1	1	0
85.4	85.38	−.02	0	0	1	1	1	1
88.5	88.61	+.13	0	1	1	1	0	0
91.5	91.58	+.09	1	1	0	1	1	1
94.8	94.76	−.04	1	0	1	1	1	0
97.4	97.29	−0.11	0	1	0	1	1	1
100.0	99.96	−.04	1	0	1	1	0	0
103.5	103.43	−.07	0	0	1	1	1	0
107.2	107.15	−.05	0	0	1	1	0	0
110.9	110.77	−.12	1	1	0	1	1	0
114.8	114.64	−.14	1	1	0	1	0	0
118.8	118.80	0.0	0	1	0	1	1	0
123.0	122.80	−.17	0	1	0	1	0	0
127.3	127.08	−.17	1	0	0	1	1	0
131.8	131.67	−.10	1	0	0	1	0	0
136.5	136.61	+.08	0	0	0	1	1	0
141.3	141.32	+.02	0	0	0	1	0	0
146.2	146.37	+.12	1	1	1	0	1	0
151.4	151.09	−.20	1	1	1	0	0	0
156.7	156.88	+.11	0	1	1	0	1	0
162.2	162.31	+.07	0	1	1	0	0	0
167.9	168.14	+.14	1	0	1	0	1	0
173.8	173.48	−.19	1	0	1	0	0	0
179.9	180.15	+.14	0	0	1	0	1	0
186.2	186.29	+.05	0	0	1	0	0	0
192.8	192.86	+.03	1	1	0	0	1	0
203.5	203.65	+.07	1	1	0	0	0	0
210.7	210.17	−.25	0	1	0	0	1	0
218.1	218.58	+.22	0	1	0	0	0	0
225.7	226.12	+.18	1	0	0	0	1	0
233.6	234.19	+.25	1	0	0	0	0	0
241.8	241.08	−.30	0	0	0	0	1	0
250.3	250.28	−.01	0	0	0	0	0	0

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		−0.3V to 7.0V
Input voltage at any pin (ref VSS = OV)		−0.3V to (VDD + 0.3V)
Output sink/source current (total)		20mA
Operating temperature range	FX335	−30°C to +85°C
	FX335L	−30°C to +70°C
Storage temperature range	FX335	−55°C to 125°C
	FX335L	−40°C to +85°C
Maximum device dissipation		100mW

Operating Limits

VDD = 5V, T_A = 25°C, O = 1MHz, Δfo = 0.
All characteristics measured using the standard test circuit (figure 3) with the following test parameters, and is valid for all tones unless otherwise stated:—

OdB reference = 300mVrms
Composite input signal = OdB 1kHz tone
−12dB noise (band limited 6kHz gaussian white noise)
−20dB fo CTCSS tone

Characteristic	See Note	Min	Typ	Max	Unit
Static Characteristics					
Supply volts		4.5	5.0	5.5	V
Supply current (decoding)			2.5	—	mA
Supply current (transmitting)			3.5	—	mA
Supply current (standby)			0.6	—	mA
Signal input impedance			3	—	MΩ
Audio output impedance			3	—	kΩ
Input impedance	1	—	500	—	kΩ
Input logic '1'	1	3.5	—	—	V
Input logic '0'	1	—	—	1.5	V
Logic '1' output I'source = 0.1mA	2	4.0	—	—	V
Logic 'O' output I'sink = 0.1 mA	2	—	—	1.0	V
Dynamic Characteristics					
Decoder					
Decode input signal level	3	−20	—	—	dB
Decode response time	3,6	—	—	250	ms
Deresponse time	3,6	—	—	250	ms
Decode selectivity	3	± 0.5	—	± 3	%fo
Encoder					
Tone output level (relative 775mVrms)		−3	0	—	dB
Tone frequency accuracy (Δfo error)			± 0.3	—	%fo
Risetime to 90% nominal o/p: fo> 100 Hz	4	—	15	—	ms
fo< 100 Hz	4	—	45	—	ms
Tone output load current		—	—	5	mA
Total harmonic distortion		—	2	5	%
Output level variation between tones		—	0.1	—	dB
Audio Filter					
Total harmonic distortion	5	—	2	5	%
Output noise level (input a.c. short citcuit, audio switch enabled)	—	—	−60	−50	dB
Audio Filter (fo < 186Hz)					
Cutoff frequency	—	—	300	—	Hz
Bandpass ripple (300 — 3.4kHz)	5	−2	—	+2	dB
Stopband attenuation (f < 186Hz)	5	36	40	—	dB
Passband gain at 1kHz		−3	−2	—	dB
Audio Filter (fo > 186Hz)					
Cutoff frequency	—	—	410	—	Hz
Bandpass ripple (410 — 3.4kHz)	5	−2	—	+2	dB
Stopband attenuation (f < 250Hz)	5	36	40	—	dB
Passband gain at 1kHz	—	−3	−2	—	dB
Audio switch					
Isolation	5	—	60	—	dB

Notes

1. *Refers to Decode Enable, Tx Enable, PTL, Decode Comparator Input, D0, D1, D2, D3, D4, D5.*
2. *Tone Decoder and Detector Outputs.*
3. *Composite Signal Test Condition.*
4. *Any programme tone and R_L = 600Ω, C_L = 15pF.*
5. *1kHz Reference = 0dB.*
6. *fo ⩾ 100 Hz, (for 100 Hz > fo > 67 Hz:*

$$t = \frac{100}{fo\ (Hz)} \times 250ms).$$

Typical Performance

Decoder Operation

The detection of the CTCSS tone is achieved in four separate stages illustrated in *Figure 1.* The signal is initially filtered by switched capacitor elements tuned to the programmed code. The output is then fed to a limiter to convert it to logic levels. The period of each logic pulse is measured by digital techniques and the resultant outputs are used to set or reset the Detector Output latch.

The Detector Output requires further processing by external integration to ensure correct operation. The integral voltage is input at the Decode Comparator pin for comparison with a reference level. An input voltage more positive than the reference level switches the Tone Decoder Output low and enables the audio switch. *Figure 4* shows a typical response sequence. Note that a logic 1 at the Decode Enable pin forces the Audio Output to a d.c. bias level. The correct CTCSS tone is assumed applied to the Signal Input.

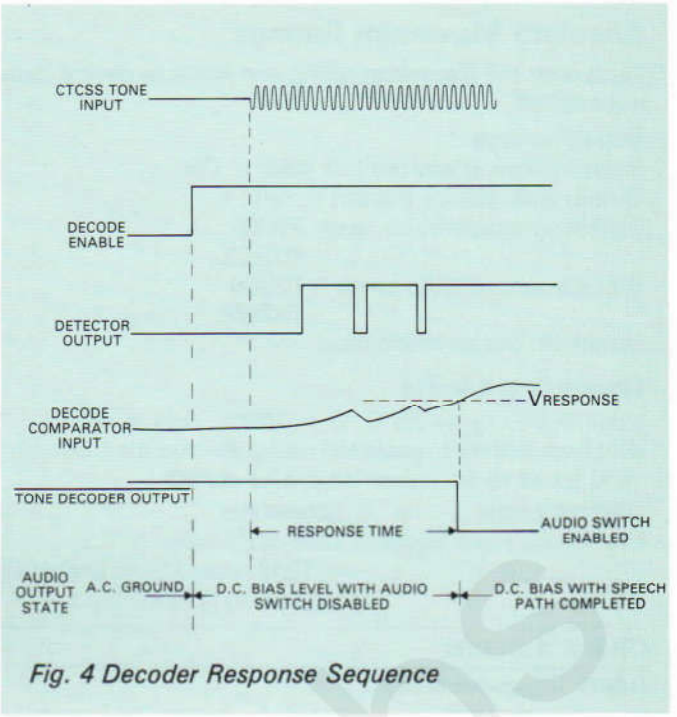


Fig. 4 Decoder Response Sequence

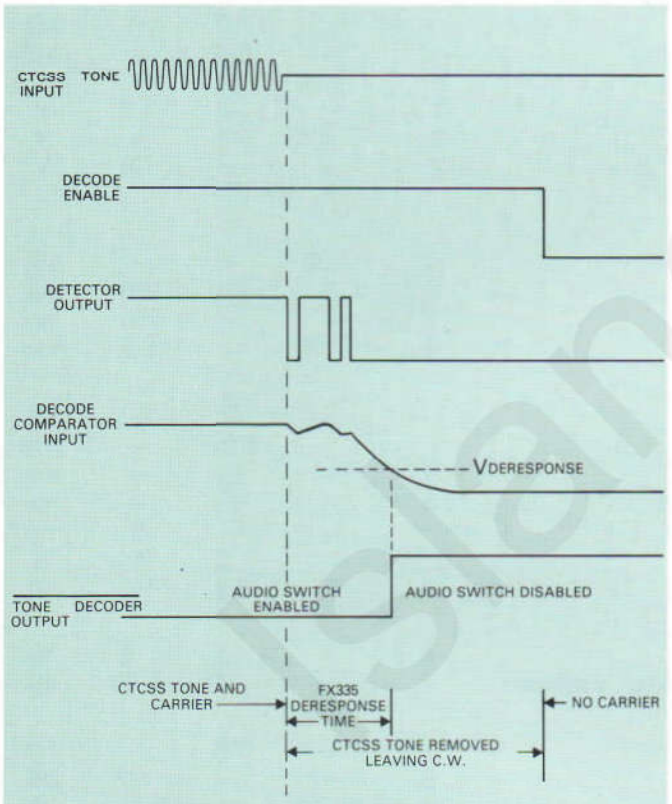


Fig. 5 Decoder Deresponse Sequence

The deresponse shown in *Figure 5* assumes the CTCSS tone is removed prior to the carrier drop out as indicated. This allows deresponse to be achieved with an unmodulated carrier ensuring a quiet shutdown.

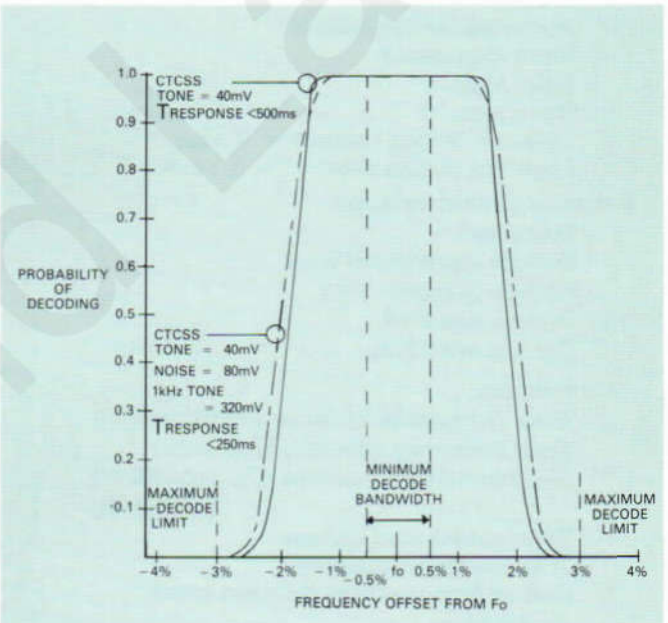


Fig. 6 Decoder Probability Curves

The characteristics of *Figure 6* show typical decode probabilities against input frequency.

Encoder Operation

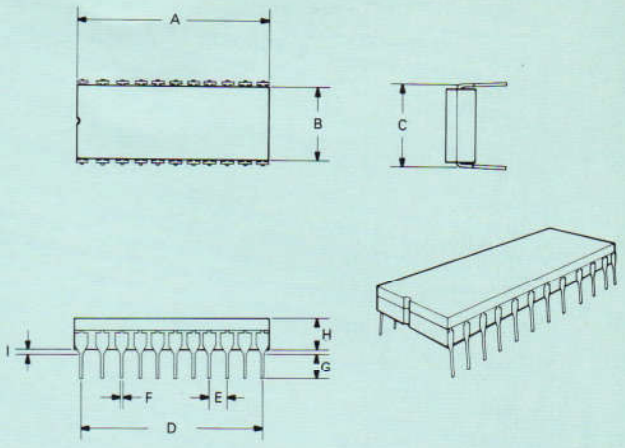
A low distortion sinewave is generated at the Tx. Tone Output when the $\overline{\text{Tx. Enable}}$ Input is activated. The emitter follower output stage can source 1mW directly into a 600 ohm load.

Package Outlines

The cerdip package of the FX335 is shown in *Figure 7.* The plastic encapsulated FX335L of *Figure 8* is supplied in the disposable carrier depicted in *Figure 9* for handling convenience.

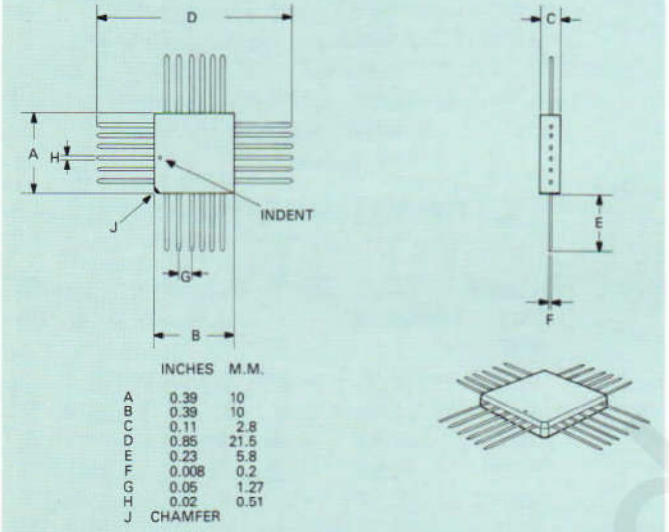
The FX335L has an indent (spot) adjacent to Pin 1 and a chamfered corner between Pins 3 and 4 to allow complete identification. Pins number counter clockwise when viewed from the top (indent side).

The carrier permits testing and handling of devices prior to assembly.



	INCHES	M.M.
A	1.08	27.4
B	0.38	9.65
C	0.42	10.7
D	1.0	25.4
E	0.1	2.54
F	0.02	0.51
G	0.13	3.3
H	0.16	4.1
I	0.03	0.76

Fig. 7 FX335 Package Outline



	INCHES	M.M.
A	0.39	10
B	0.39	10
C	0.11	2.8
D	0.85	21.5
E	0.23	5.8
F	0.008	0.2
G	0.05	1.27
H	0.02	0.51
J	CHAMFER	

Fig. 8 FX335L Package Outline

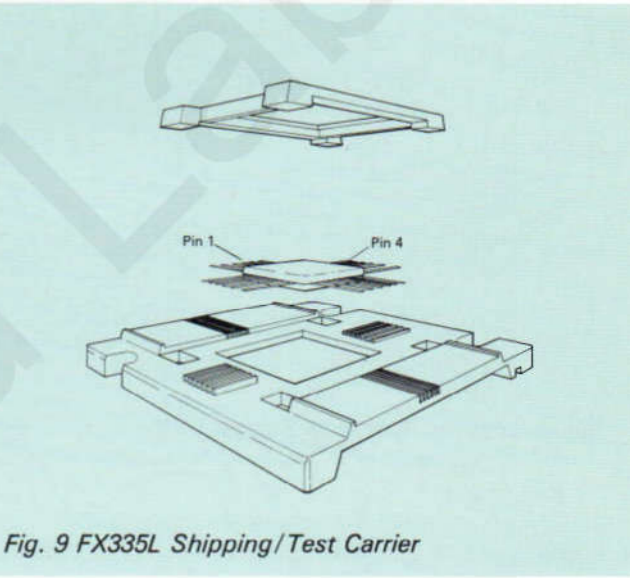


Fig. 9 FX335L Shipping/Test Carrier

Handling Precautions

The FX335/L is a CMOS LSI integrated circuit which includes input protection. However, precautions should be taken to prevent static discharges which can cause damage.

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