



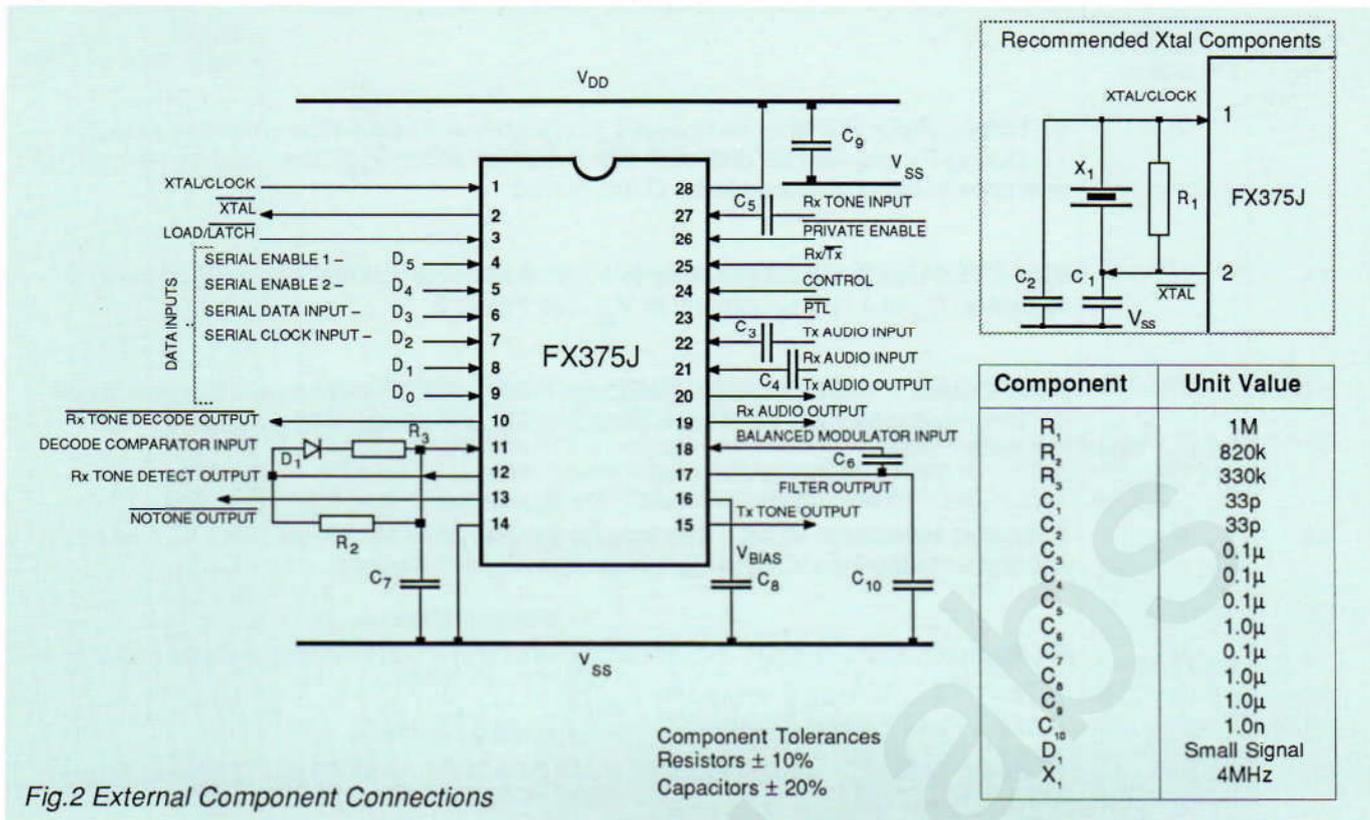
**Pin Number**      **Function**

DIL FX375J	PLCC FX375LH	
1	1	<b>Xtal/Clock:</b> The input to the clock oscillator inverter. An external 4MHz Xtal or clock input is to be applied at this pin. See Figure 2.
2	2	<b>Xtal:</b> The 4MHz output of the clock oscillator inverter. See Figure 2.
3	3	<b>Load/Latch:</b> This input regulates the operation of the eight input latches : $D_0, D_1, D_2, D_3, D_4, D_5, \overline{Rx/Tx}$ and <u>Private Enable</u> for both parallel and serial input load modes. $\overline{Rx/Tx}$ and <u>Private Enable</u> inputs can be used independently in either mode by the use of Load/Latch and Control inputs configured as shown in Table 3, the data format ( $D_0 - D_5$ ), remains as set. This input has an internal $1M\Omega$ pullup resistor.
4	4	<b><math>D_5</math> - (Serial Enable 1) :</b>
5	5	<b><math>D_4</math> - (Serial Enable 2) :</b> The $\overline{Rx/Tx}$ tone programming and function inputs. Programmed as shown in Table 2 these inputs will select the CTCSS tone frequency and parallel or serial loading function. Notone, when set in receive, enables the Rx
6	6	<b><math>D_3</math> - (Serial Data Input) :</b> Audio Output and forces the Rx Tone Decode Output to a logic '0,' in transmit the Tx Tone Output is held at $V_{BIAS}$ (Notone). These inputs each have an internal $1M\Omega$ pullup resistor.
7	7	<b><math>D_2</math> - (Serial Clock Input) :</b>
8	8	<b><math>D_1</math></b>
9	9	<b><math>D_0</math></b>
10	10	<b>Rx Tone Decode Output :</b> The output of the decode comparator. In Rx a logic '0' indicates 'CTCSS tone decoded' above the internal reference level, or Notone programmed. This action internally enables the Rx audio path and Frequency Inversion function (when applicable) as shown in Table 1. In Tx this output is a logic '1'.
11	11	<b>Decode Comparator Input :</b> A logic '1' at this pin, in Rx, is compared internally with a fixed reference level, a more positive input value will produce a logic '0' at the Rx Tone Decode Output. This input should be externally connected to the Rx Tone Detect Output via external integrator components $C_7, R_2, R_3, D_1$ (see Figure 2).
12	12	<b>Rx Tone Detect Output :</b> This output, in Rx, goes to a logic '1' when a valid, programmed CTCSS tone is received at the Rx Tone Input. This input should be externally connected to the Decode Comparator Input via external integrator components $C_7, R_2, R_3, D_1$ (see Figure 2).
13	13	<b>Notone Output :</b> Outputs a logic '0' when a " Notone" CTCSS code has been programmed . It can be used to operate squelch circuitry under receive "Notone" conditions.
14	14	<b><math>V_{SS}</math> :</b> Negative supply rail (GND).

## Pin Number      Function

DIL FX375J	PLCC FX375LH	
15	15	<b>Tx Tone Output</b> : This is the buffered, programmed CTCSS tone sinewave output in Tx. During Rx and Notone operation this output is held at $V_{BIAS}$ . See note "g," page 7 with reference to capacitive load limits of this output.
16	16	$V_{BIAS}$ : This bias pin is set internally to $V_{DD}/2$ . It must be externally decoupled using a capacitor, $C_8$ , of 1.0 $\mu$ F (minimum) to $V_{SS}$ , see Figure 2.
17	17	<b>Filter Output</b> : The Input Audio Bandpass Filter output, this pin must be connected to the Balanced Modulator Input via a capacitor, $C_8$ , and decoupled to $V_{SS}$ by $C_{10}$ , see Figure 2.
18	18	<b>Balanced Modulator Input</b> : The input to the Balanced Modulator, this pin must be connected to the Filter Output via a capacitor, $C_8$ , see Figure 2.
19	19	<b>Rx Audio Output</b> : Outputs the received audio from a buffered output stage and is held at $V_{BIAS}$ when in Tx.
20	20	<b>Tx Audio Output</b> : The output of the audio path in the Tx mode and is held at $V_{BIAS}$ when in Rx.
21	21	<b>Rx Audio Input</b> : The Audio input pin for the Rx mode. Input signals should be a.c. coupled via an external capacitor, $C_4$ , see Figure 2.
22	22	<b>Tx Audio Input</b> : This is the voice input pin for the Tx mode. Signals should be a.c. coupled via an external capacitor, $C_3$ , see Figure 2.
23	23	<b>PTL</b> : The "Press To Listen" function input, in the receive mode a logic '0' enables the Rx Audio Output directly, overriding tone squelch but not intercepting a private conversation. In the transmit mode a logic '0' reverses the phase of the Tx Tone Output for "squelch tail" reduction (see Table 1), this function, in Tx, should be accurately applied by a timing circuit to ensure correct system operation.
24	24	<b>Control</b> : This input, with Load/Latch, selects the operational mode of Rx/Tx and Private Enable functions, see Table 3.
25	25	<b>Rx/Tx</b> : Selects the receive or transmit mode (Rx = '1', Tx = '0') and can be loaded by serial or parallel means, as described in Table 3.
26	26	<b>Private Enable</b> : This input selects either Private or Clear modes (Clear = '1', Private = '0'), and can be loaded by serial or parallel means, as described in Table 3. In Rx this input could be taken from the Rx Tone Decode Output. This input has an internal 1M $\Omega$ pullup resistor.
27	27	<b>Rx Tone Input</b> : The received tone input to the on-chip CTCSS decoder and should be a.c. coupled via capacitor $C_5$ , see Figure 2.
28	28	$V_{DD}$ : Positive supply rail. A single +5V power supply is required.

# Operational Information



Recommended Xtal Components

Component	Unit Value
R <sub>1</sub>	1M
R <sub>2</sub>	820k
R <sub>3</sub>	330k
C <sub>1</sub>	33p
C <sub>2</sub>	33p
C <sub>3</sub>	0.1 $\mu$
C <sub>4</sub>	0.1 $\mu$
C <sub>5</sub>	0.1 $\mu$
C <sub>6</sub>	1.0 $\mu$
C <sub>7</sub>	0.1 $\mu$
C <sub>8</sub>	1.0 $\mu$
C <sub>9</sub>	1.0 $\mu$
C <sub>10</sub>	1.0n
D <sub>1</sub>	Small Signal
X <sub>1</sub>	4MHz

Fig.2 External Component Connections

**Operational Truth Table** – Table 1 (below) illustrates the output paths and logic functions of the FX375 Private Squelch Circuit in both Receive and Transmit modes.

Receive Operation – (Rx/Tx = '1')							
In the Rx mode Tx Tone and Tx Audio paths are held at bias.							
D <sub>0</sub> – D <sub>5</sub>	Notone	Private Enable	PTL	Rx Tone Detect	Rx Tone Decode	Receive Signal Path State	Receive Signal Path Condition
Tone	1	0	1	0	1	bias	X
Tone	1	0	0	0	1	open	Not Inverted
Tone	1	0	X	1	0	open	Inverted
Notone	0	0	X	X	0	open	Not Inverted
Tone	1	1	1	0	1	bias	X
Tone	1	1	0	0	1	open	Not Inverted
Tone	1	1	X	1	0	open	Not Inverted
Notone	0	1	X	X	0	open	Not Inverted
Transmit Operation – (Rx/Tx = '0')							
In the Tx mode the Rx audio path is held at bias and the Rx Tone Detect output at logic '0'.							
D <sub>0</sub> – D <sub>5</sub>	Notone	Private Enable	PTL	Transmitted Tone State	Transmitted Tone Phase	Transmit Signal Path State	Transmit Signal Path Condition
Tone	1	0	1	active	0°	open	Inverted
Tone	1	0	0	active	180°	open	Inverted
Notone	0	0	X	bias	X	open	Not Inverted
Tone	1	1	1	active	0°	open	Not Inverted
Tone	1	1	0	active	180°	open	Not Inverted
Notone	0	1	X	bias	X	open	Not Inverted

**Notes**

1. The pre- and de-emphasis circuits remain in the Transmit path during Clear and Private operation.
2. Power remains applied to the CTCSS tone decoder at all times.
3. Carrier Frequency = 3333Hz during Private operation (Tx or Rx).
4. During Clear operation the carrier frequency is turned off to reduce spurious emissions.
5. Under Rx-Notone conditions the Notone output can be used to operate squelch circuitry.
6. The functions in this table are applicable when the device is connected as recommended in Figure 2.

Table 1 Functions and Outputs

## Operational Information

The logical inputs ( $D_0 - D_5$ ) are used to programme the FX375 tone frequency ( $Rx/Tx$ ) as shown in Table 2 (below). Loading of data is carried out in either serial or parallel formats.

Nominal Frequency (Hz)	FX375 Frequency (Hz)	$\Delta f_0$ (%)	Tone Data Programme Inputs					
			$D_0$	$D_1$	$D_2$	$D_3$	$D_4$	$D_5$
67.0	67.05	+ 0.07	1	1	1	1	1	1
71.9	71.9	0	1	1	1	1	1	0
74.4	74.35	- 0.07	0	1	1	1	1	1
77.0	76.96	- 0.5	1	1	1	1	0	0
79.7	79.77	+ 0.09	1	0	1	1	1	1
82.5	82.59	+ 0.1	0	1	1	1	1	0
85.4	85.38	- 0.2	0	0	1	1	1	1
88.5	88.61	+ 0.13	0	1	1	1	0	0
91.5	91.58	+ 0.09	1	1	0	1	1	1
94.8	94.76	- 0.04	1	0	1	1	1	0
97.4	97.29	- 0.11	0	1	0	1	1	1
100.0	99.96	- 0.04	1	0	1	1	0	0
103.5	103.43	- 0.07	0	0	1	1	1	0
107.2	107.15	- 0.05	0	0	1	1	0	0
110.9	110.77	- 0.12	1	1	0	1	1	0
114.8	114.64	- 0.14	1	1	0	1	0	0
118.8	118.8	0	0	1	0	1	1	0
123.0	122.8	- 0.17	0	1	0	1	0	0
127.3	127.08	- 0.17	1	0	0	1	1	0
131.8	131.67	- 0.10	1	0	0	1	0	0
136.5	136.61	+ 0.08	0	0	0	1	1	0
141.3	141.32	+ 0.02	0	0	0	1	0	0
146.2	146.37	+ 0.12	1	1	1	0	1	0
151.4	151.09	- 0.2	1	1	1	0	0	0
156.7	156.88	+ 0.11	0	1	1	0	1	0
162.2	162.31	+ 0.07	0	1	1	0	0	0
167.9	168.14	+ 0.14	1	0	1	0	1	0
173.8	173.48	- 0.19	1	0	1	0	0	0
179.9	180.5	+ 0.14	0	0	1	0	1	0
186.2	186.29	+ 0.05	0	0	1	0	0	0
192.8	192.86	+ 0.03	1	1	0	0	1	0
203.5	203.65	+ 0.07	1	1	0	0	0	0
210.7	210.17	- 0.25	0	1	0	0	1	0
218.1	218.58	+ 0.22	0	1	0	0	0	0
225.7	226.12	+ 0.18	1	0	0	0	1	0
233.6	234.19	+ 0.25	1	0	0	0	0	0
241.8	241.08	- 0.30	0	0	0	0	1	0
250.3	250.28	- 0.01	0	0	0	0	0	0
Serial Input Mode			X	X	Clk	Data	0	1
Notone			0	0	0	0	1	1

Table 2 Tone Programming

**Load/Latch and Control Functions** – The Load/Latch function regulates the loading of the FX375 tone frequency ( $D_0 - D_5$ , Table 2) in either the serial or parallel modes. The Control input enables the flexible use of the Rx/Tx and Private Enable functions, its use is illustrated in Table 3.

Load Configuration	Load/Latch Logic	and	Control Logic	Loading mode of :-	
				$D_0 - D_5$	Rx/Tx, Private Enable
Parallel	1		0	Transparent	Transparent
Parallel	0		0	Latched	Latched
Parallel	1		1	Transparent	Transparent
Parallel	0		1	Latched	Transparent
Serial	0		1	Load data in	Transparent
Serial	0 - 1 - 0		0	Latch data in	Latched

### Notes

**Glossary** – Transparent Data at the device inputs acts directly.  
 Latched In this position data and/or functions are latched in.  
 '0 - 1 - 0' is a strobe pulse as shown in figures 3 and 4 (Timing).

Table 3 Load/Latch and Control Functions

**Timing Information .....** Control instructions are input to the FX375 by serial (figure 3) or parallel (figure 4) means, using Data Inputs and Load/Latch as shown in the diagrams below.

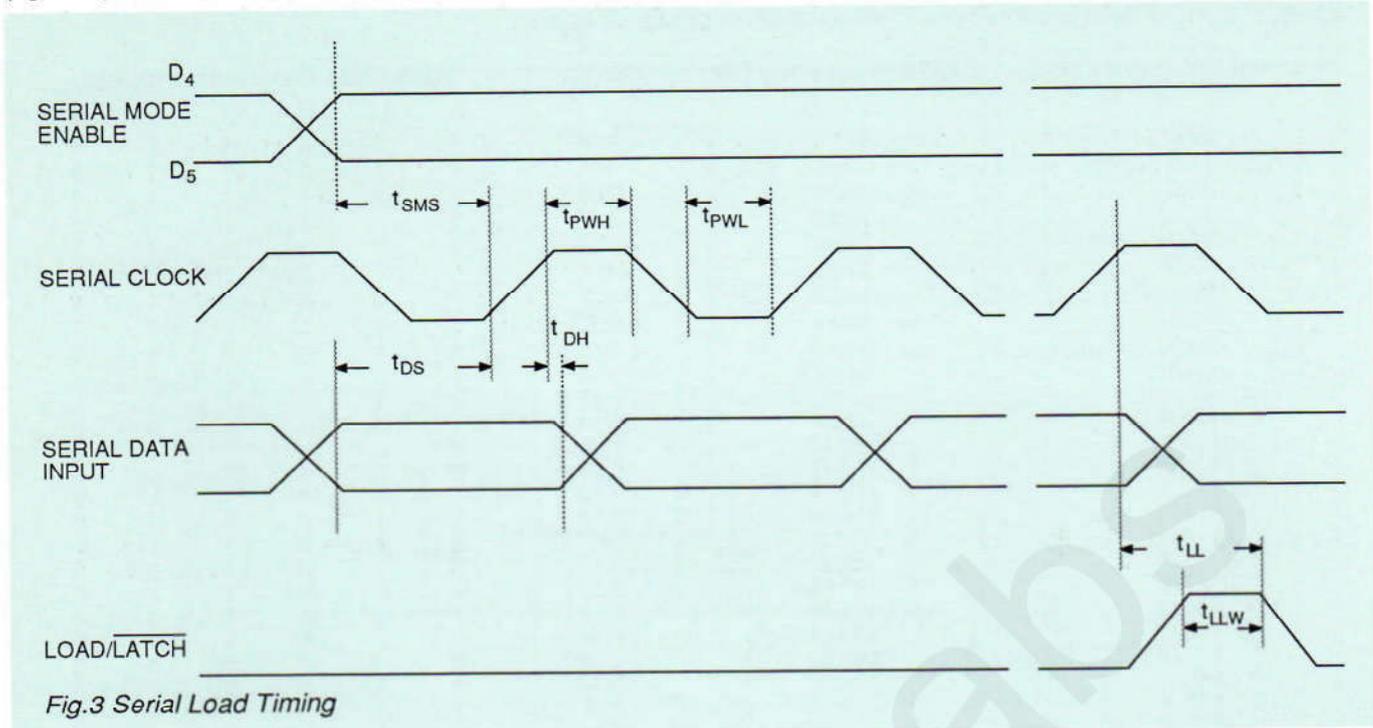


Fig.3 Serial Load Timing

	Min.	Typ.	Max.	Unit
<b>Serial</b>				
Serial Mode Enable Set Up Time - ( $t_{SMS}$ )	250	-	-	ns
Clock 'High' Pulse Width - ( $t_{PWH}$ )	250	-	-	ns
Clock 'Low' Pulse Width - ( $t_{PWL}$ )	250	-	-	ns
Data Set Up Time - ( $t_{DS}$ )	150	-	-	ns
Data Hold Time - ( $t_{DH}$ )	50	-	-	ns
Load/Latch Set Up Time - ( $t_{LL}$ )	250	-	-	ns
Load/Latch Pulse Width - ( $t_{LLW}$ )	150	-	-	ns
<b>Parallel</b>				
Data Valid Time - ( $t_{VP}$ )	200	-	-	ns
Load Time - ( $t_L$ )	150	-	-	ns
Fall Time - ( $t_F$ )	-	-	50	ns
Data Hold Time - ( $t_H$ )	50	-	-	ns

**Serial Loading Sequence :** With Load/Latch at logic '0' serial data is loaded in the sequence :-  $D_5, D_4, D_3, D_2, D_1, D_0, Rx/Tx, Private Enable$ . When these 8 bits have been clocked in on the rising clock edge, data is latched by strobing the Load/Latch input - "0-1-0" (Figure 3).

Table 4 Timing

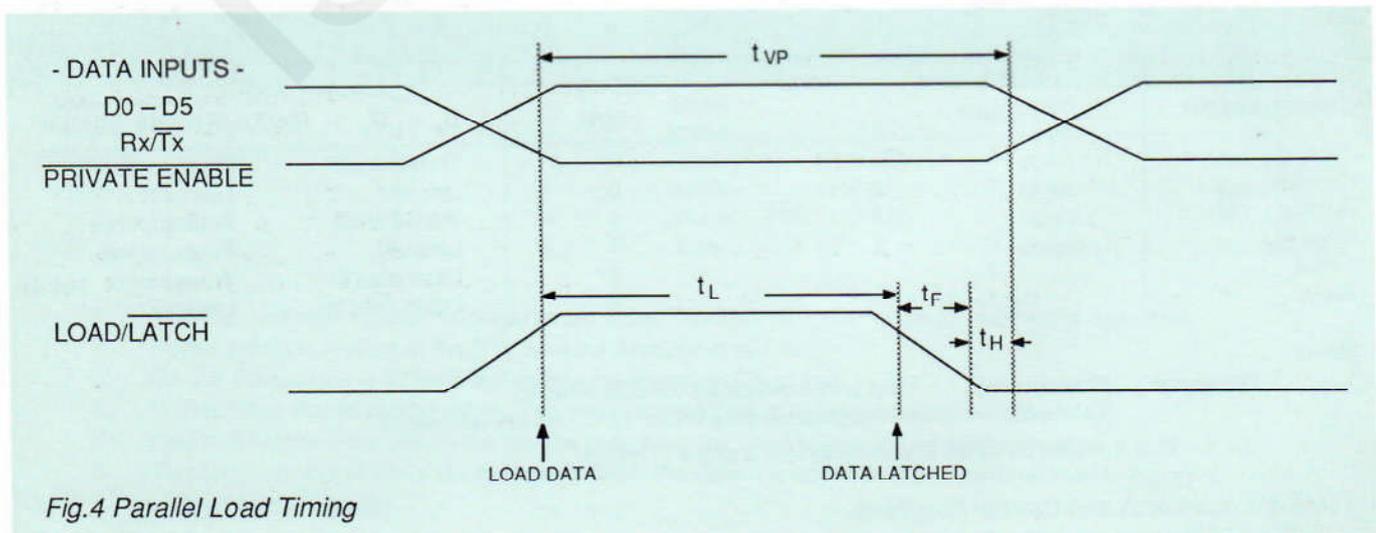


Fig.4 Parallel Load Timing

## Specification

## Electrical Characteristics

### Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage	- 0.3 to 7.0V
Input voltage at any pin (ref $V_{SS} = 0V$ )	- 0.3 to ( $V_{DD} + 0.3V$ )
Sink/source current (supply pins)	+/- 30mA
(other pins)	+/- 20mA
Total device dissipation @ $T_{AMB} = 25^{\circ}C$	800mW Max.
Derating	10mW/ $^{\circ}C$
Operating temperature range: <b>FX375J</b>	- 30 $^{\circ}C$ to + 85 $^{\circ}C$ (ceramic)
<b>FX375LH</b>	- 30 $^{\circ}C$ to + 70 $^{\circ}C$ (plastic)
Storage temperature range: <b>FX375J</b>	- 55 $^{\circ}C$ to + 125 $^{\circ}C$ (ceramic)
<b>FX375LH</b>	- 40 $^{\circ}C$ to + 85 $^{\circ}C$ (plastic)

### Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

$V_{DD} = 5.0V$ ,  $T_{AMB} = 25^{\circ}C$ , Xtal/Clock  $f_0 = 4.0$  MHz, Audio level 0dB ref: = 300mV rms.

Composite input signal = 0dB, 1kHz tone in -12dB (6kHz band limited) gaussian white noise with a -20dB CTCSS tone.

Characteristics	See Note	Min.	Typ.	Max.	Unit
<b>Static Values</b>					
Supply Voltage		4.5	5.0	5.5	V
Supply Current :					
Rx /Tx (Operating)		-	8.0	-	mA
Rx standby (No Decode)		-	2.8	-	mA
Rx only (Decoding)		-	5.0	-	mA
Analogue Input Impedance		-	0.5	-	M $\Omega$
Analogue Output Impedance		-	0.5	-	k $\Omega$
Tone Input Impedance		-	1.0	-	M $\Omega$
Digital Input Impedance		-	1.0	-	M $\Omega$
Input Logic '1'		3.5	-	-	V
Input Logic '0'		-	-	1.5	V
Output Logic '1' (I = 0.1mA)		4.0	-	-	V
Output Logic '0' (I = 0.1mA)		-	-	1.0	V
<b>Dynamic Values</b>					
Maximum Input Level		-	+ 10.5	-	dB
<b>Decoder</b>					
Tone Input Signal Level	1,4	- 20	-	-	dB
Response Time	1,4,6	-	-	250	ms
De-response Time	1,4,6	-	-	250	ms
Selectivity	4	$\pm 0.5$	-	$\pm 3.0$	%fo
<b>Encoder</b>					
Tone Output Level (relative 775mVrms)		- 3.0	0	+ 3.0	dB
Tone Frequency Accuracy		- 0.3	-	+ 0.3	%fo
Tone Harmonic Distortion		-	2.0	5.0	%
Tone Output Load Current	2	-	-	5.0	mA
Output Level Variation between Tones		-	0.1	-	dB
Rise Time (to 90% nominal level)					
(fo > 100Hz)	5	-	15	-	ms
(fo < 100Hz)	5	-	45	-	ms

Characteristics	See Note	Min.	Typ.	Max.	Unit
<b>Rx Clear</b>					
Total Harmonic Distortion	3	-	2	5	%
Output Noise Level	7	-	-43	-	dB
Passband Gain (300Hz – 3033Hz)		-	0	-	dB
Passband Ripple (300Hz – 3033Hz)	3	-	-	3	dB
Audio Stopband Attenuation ( $f_{in} > 3333\text{Hz}$ )		-	20	-	dB
( $f_{in} > 3633\text{Hz}$ )		-	45	-	dB
( $f_{in} < 250\text{Hz}$ )		-	42	-	dB
<b>Rx Invert</b>					
Carrier Frequency		-	3333	-	Hz
Total Harmonic Distortion	3,8	-	4	10	%
Baseband Breakthrough		-	-40	-	dB
Carrier Breakthrough		-	-40	-	dB
Output Noise Level	7	-	-37	-	dB
Passband Ripple (300Hz – 3033Hz)	8	-	-	5	dB
Audio Stopband Attenuation ( $f_{in} > 3333\text{Hz}$ )		-	50	-	dB
( $f_{in} > 3633\text{Hz}$ )		-	60	-	dB
( $f_{in} < 250\text{Hz}$ )		-	60	-	dB
<b>Tx Clear</b>					
Total Harmonic Distortion	3	-	3	5	%
Output Noise Level	7	-	-43	-	dB
Passband Gain (300Hz – 3033Hz)	3	-	0	-	dB
Passband Ripple (300Hz – 3033Hz)	3	-	-	4	dB
Audio Stopband Attenuation ( $f_{in} > 3333\text{Hz}$ )		-	20	-	dB
( $f_{in} > 3633\text{Hz}$ )		-	45	-	dB
( $f_{in} < 250\text{Hz}$ )		-	42	-	dB
Pre- and De-emphasis		-	-	6	dB/octave
<b>Tx Invert</b>					
Carrier Frequency		-	3333	-	Hz
Total Harmonic Distortion	3,8	-	4	10	%
Baseband Breakthrough		-	-40	-	dB
Carrier Breakthrough		-	-40	-	dB
Output Noise Level	7	-	-37	-	dB
Passband Ripple (300Hz – 3033Hz)	3,8	-	-	5	dB
Audio Stopband Attenuation ( $f_{in} > 3333\text{Hz}$ )	8	-	50	-	dB
( $f_{in} > 3633\text{Hz}$ )	8	-	60	-	dB
( $f_{in} < 250\text{Hz}$ )	8	-	60	-	dB
Pre- and De-emphasis		-	-	6	dB/octave

Notes

1. These values are obtained using the external integrator components as detailed in Figure 2.
2. An Emitter Follower output.
3. With an input signal of 1kHz @ 0dB.
4. Under Composite Signal test conditions.
5. Any programmed tone with  $RL = 600$ ,  $CL = 15\text{pF}$ . Including any response to a phase reversal instruction.
6.  $f_o > 100\text{Hz}$ , (for  $100\text{Hz} > f_o > 67\text{Hz}$  :  $t = [100/f_o \text{ (Hz)}] \times 250\text{ms}$ ).
7. Input a.c. short circuit, audio path enabled, measured in a 30kHz bandwidth.
8. Due to frequency inversion, this figures reflects the difference from the expected ideal response.

## Private Squelch Circuit ..... Application Notes

The FX375 Private Squelch Circuit utilizes Audio Frequency Inversion and Continuous Tone Controlled Squelch System (CTCSS) techniques to provide secure voice communication on a common radio channel.

**Clear/Private Switching** is controlled by the logic state of the Private Enable input. Table 1 shows that, in the receive condition the signal path will only be inverted when the programmed CTCSS tone is received. Although other logic actions will enable the receive path, privacy of the conversation is maintained at all times.

**Pre- and De-emphasis** (6dB/octave) filters are included on-chip in the transmit path, so that the use of this device will produce natural sounding audio (clear or private modes) when installed in modern radio communication transceivers, with or without existing audio processing circuitry. The recommended layout is shown in block form below.

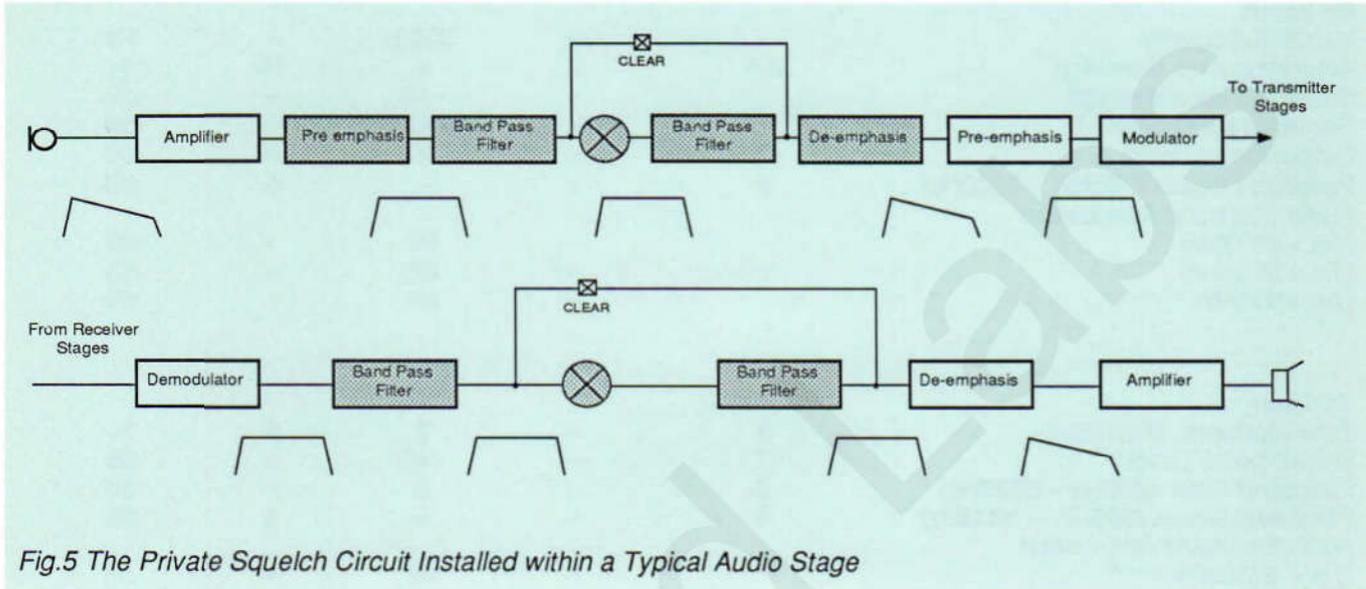


Fig.5 The Private Squelch Circuit Installed within a Typical Audio Stage

Figure 5 shows the recommended positioning of the FX375 (shaded areas) when installed within the audio stages of a typical transceiver system. The accompanying waveform diagrams indicate the relative "voice band amplitudes" at each stage of the receive or transmit process.

**Installation Recommendations** – Care should be taken on the design and layout of the printed circuit board taking into consideration the points noted below.

- All external components (as recommended in Figure 2) should be kept close to the package.
- Tracks should be kept short, particularly the Audio and  $V_{BIAS}$  inputs.
- Xtal/clock and digital tracks should be kept well away from analogue inputs and outputs.
- Inputs and outputs should be screened wherever possible.
- A "ground plane" connected to  $V_{SS}$  will assist in eliminating external pick-up on input and output pins.
- It is recommended that the power supply rails have less than 1mV rms of noise allowed.
- Tx Tone Output loading – Large capacitive loads could cause this pin to oscillate. If capacitive loads in excess of 100pF are unavoidable, a resistor of 1k $\Omega$  or greater put in series with the load should minimise this effect.

## Package Outline

The FX375J, the cerdip package is shown in Figure 10, and the 'LH' version in Figure 11. To allow complete identification, the 'LH' package has an indent spot adjacent to pin 1 and a chamfered corner between pins 4 and 5. Pins number anti-clockwise when viewed from the top (indent side).

## Handling Precautions

The FX375 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

Fig.10 FX375J DIL Package

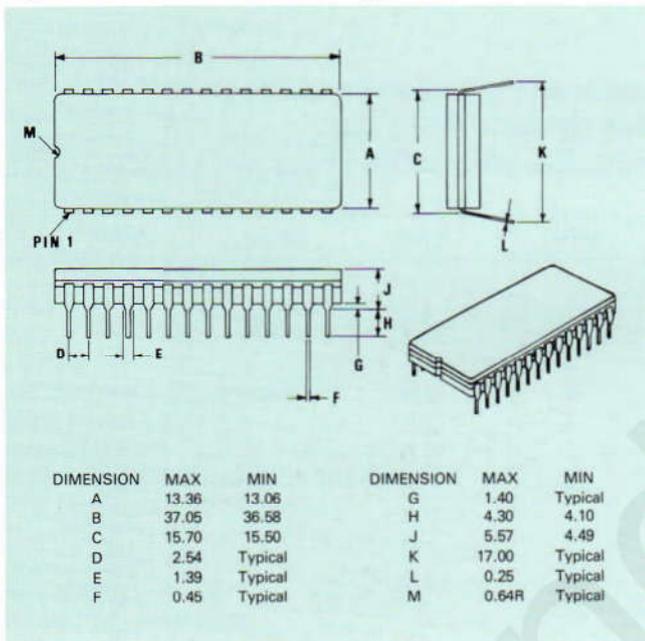
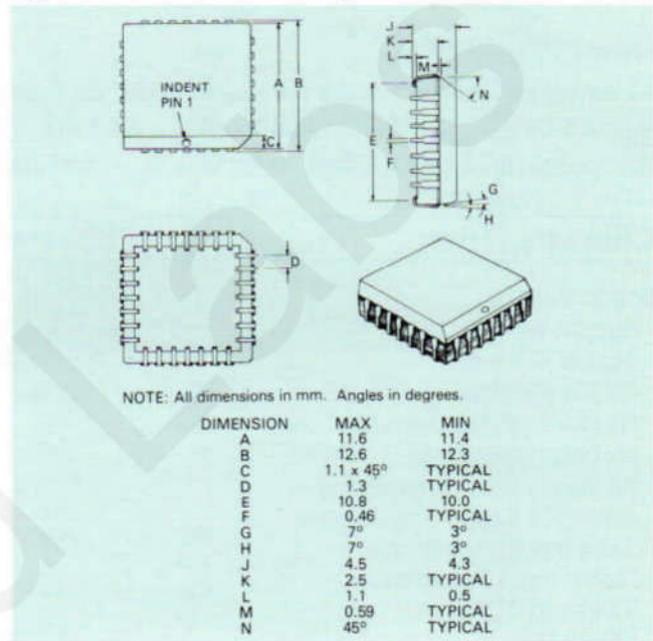


Fig.11 FX375LH Package



## Ordering Information

<b>FX375J</b>	<b>28-pin cerdip DIL</b>
<b>FX375LH</b>	<b>28-lead plastic leaded chip carrier</b>

CML does not assume any responsibility for the use of any circuitry described. No circuit patent licences are implied and CML reserves the right at any time without notice to change the said circuitry.



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